Contribution to Digital System Testing Methods

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Abstract

System-on-chip is an integrated circuit comprising of numerous functional cores which can be of various types. Testing of such diverse circuit is very complex problem. Test access to digital cores is ensured by core wrapper architectures. The paper presents two novel contributions to core test wrappers: (1) the set of optimization techniques for parallel interface to provide faster test application and (2) effective method of delay fault test generation requiring only the simple test wrapper architecture.

Categories and Subject Descriptors

B.7.3 [**Reliability and Testing**]: Test generation

Keywords

system-on-chip, test wrapper architectures, test generation, delay test, skewed-load test

1. Introduction

Integrated circuits technologies are very fast growing industry. According to expert studies the number of transistors integrated on a single chip is growing every year rapidly [3]. The number of functional blocks that can be implemented on a chip is increasing as well. Such whole systems integrated on chip (SoC — System-on-Chip) contain different types of memories and functional blocks (cores), which are mostly provided by different vendors/designers. The most currently used technology in practice is CMOS [3]. The nanometers technology structures are nowadays supplied with low power. Therefore, a voltage difference between logic values decreases rapidly, new defects appear, and the total yield is reducing in the device production.

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Testing of integrated circuits has always been a very important area of applied informatics [8]. Role of testing is to increase the production yield and also to ensure a satisfactory lifetime of integrated circuits. Testing of digital circuits in the past was focused on methods and efficient test generation algorithms, later on automatic testing of digital circuit (e.g. BIST — Build-in Self Test) and design of easy-testable sequential circuits using various scan methods. However, with the SoC platform increase new problems need to be solved.

Testing of a complex SoC system with different and often deeply embedded logic cores and memories faces new test requirements. The embedded cores are not accessible from primary ports, and therefore design methods were developed to improve their testability [8]. The conceptual architecture for the core test distinguishes three basic elements [24]:

- Test pattern source and sink — a test pattern source generates test vectors and a sink stores and/or evaluates core responses.
- Test access mechanism (TAM) — on-chip test data transportation from a source to a core and from a core to a sink.
- Core test wrapper — provides controllability and observability of the core inputs/outputs and ensures the switching capability between the core and its various TAMs.

Core test wrappers are mostly designed in accordance with one of two IEEE standards: IEEE 1149.1 — Test Access Port and Boundary-Scan Architecture [1] and IEEE 1500 — Testability Method for Embedded Core-Based Integrated Circuits [2].

IEEE 1149.1 standard (known as JTAG) was developed for testing circuit boards using boundary scan. For its versatility and certain similarity between the board testing and SoC testing it is also used as the core test wrapper. IEEE 1500 standard test wrapper additionally offers optional parallel test access and simple non-state-machine control in comparison with IEEE 1149.1 standard from design view.

Beside the growing test complexity, new defects appear in latest technologies, which manifest as increased delay. If the delay is relatively small, under certain circumstances it may not occur in functional mode at all. However, even such small defects may cause failures later in the

functional lifetime. Therefore, digital circuits need to be tested also for delay faults.

Several models for delay faults have been proposed to model the different types of delay faults and based on different testing approaches. Generation and application of tests for delay fault models become a standard part of the testing procedures of digital circuits. But the generation and application of such tests for cores embedded in SoC is not a trivial problem [8].

The contribution of this thesis is improvement of the test quality of digital cores embedded in SoC with application of test vectors through the standard testability architectures. The rest of the paper is organized as follows. Motivation is presented in Section 2 and main objectives in Section 3. Section 4 describes proposed optimization techniques for parallel interface. Section 5 describes proposed method for delay fault test generation aimed at embedded cores. The paper is concluded by experimental results.

2. Motivation

The aim of the thesis was to improve the quality of testing of digital cores surrounded with test wrapper (1) by optimizing the parallel interface for faster test application and (2) by effective method of delay fault test generation requiring only the simple test wrapper architecture.

2.1 Test wrapper optimization

The size of cores embedded into SoC is growing, which results in long test sequences with long application time. Therefore, a parallel test access became a very popular test application feature. It increases the test data throughput and decreases the test application time. But these advantages are not provided automatically. When the width of the parallel TAM is not equal to the core terminals number the test wrapper may need to perform a test width adaptation. All test scan elements (input, output scan cells and internal scan chains) should be formed into the parallel scan lines of which the number is equal to the TAM width. The parallel scan lines should be balanced [9] for one of several parameters — length of lines, scan-in time and scan-out time for different test types. The proper optimization for the desired parameter has to be done.

2.2 Delay fault test generation method

Embedded digital blocks and their interconnections have to be verified by at-speed testing to satisfy the quality and reliability of nowadays SoCs. Once a chip is fabricated, it must be tested for pre-specified clock frequency and therefore testing has to also cover speed related faults.

Many delay fault models and related test generation techniques have been defined and used in digital circuits [10, 17,18]. The common feature of the most delay fault models is that test is composed of vector-pairs $< v1, v2 >$, where $v1$ is the initialization vector and $v2$ is the excitation vector for delay fault detection. The basic delay fault models are: transition fault, gate delay fault and path delay fault. The transition and the path delay fault models are the most frequently applied ones for combinational and scan-based sequential circuits. Several new models [14, 16] have been developed to use or combine some of the positive features of the basic models.

The scan chain design is the most frequently used method to increase testability of deeply embedded cores in SoC. However, using the scan-based test architectures in vector-pair testing is not a trivial problem. Test generation algorithms for combinational and scan-based synchronous circuits are well known while application techniques of tests through test wrappers are still under development.

Three basic approaches should be considered for vector-pair test application through a core's internal scan chains: skewed-load test [19], broadside test [20] and enhanced scan test. Skewed-load and broad side tests use scan chain composed of simple scan cells (one memory element per one cell). The first vector of vector-pair is shifted in like a standard test vector. Difference between these two test approaches lies in the way how to produce the second vector. Broadside test uses circuit's response and skewed-load test uses one additional shift to produce the desired excitation vector. On the other hand, enhanced scan test uses enhanced scan cells (two memory elements per one cell). The test architecture is much larger in comparison with simple scan chains but its advantage is in the capability of arbitrary vector-pairs application.

The enhanced scan cell is also used in test wrapper design to provide vector-pair test. Several approaches [21–23] deal with vector-pair application differently but none of them uses simple boundary scan chain without assistance of surrounding cores.

3. Objectives

The thesis objectives for embedded digital cores testing optimized for test application time and minimal test area in SoCs using the test wrapper architectures are:

- Development of optimization methods for the parallel test wrapper interface allowing the arrangement of scan cells and internal scan chains based on the following criteria:
  - effective application of test vectors for the core internal test,
  - effective application of test vectors for the core external test,
  - and the balance of the total length of parallel lines.
- Development of a test generation method for delay faults with primary application to test wrappers comprising simple boundary scan chains. The generated test must be applicable to the core without any assistance of neighboring test wrappers.
- Development of a methodology for the universal application of the test generation method for delay faults in a variety of test wrapper architectures.

4. New test wrapper optimization techniques

The set of single optimization techniques [4] and one reconfigurable technique were developed for parallel scan lines optimization. Subsection 4.1 describes the single optimization techniques, Subsection 4.2 describes the reconfigurable technique, and experimental results are presented in Subsection 4.3.

4.1 Single optimization techniques

Four optimization techniques have been developed for the parallel scan lines ordering [4]. Each technique can be applied on the core with the parallel interface and is targeted to internal (INTEST) or external (EXTEST) testing. The first technique is targeted to cores in which mainly the internal structure is tested. It means INTEST application time (scan-in time) and reading responses time (scan-out time) are optimized. When INTEST is performed, the test vectors are applied into input scan cells and internal scan chains. Therefore, input cells have to be ordered to the beginning of the parallel scan lines for scan-in time minimization. For scan-out time minimization, output cells are ordered at the end of the parallel scan lines. The internal scan chains are used with scan-in and scan-out procedures as well. The optimization technique distributes the scan cells and the internal scan chains to create balanced parallel lines for scan-in time and scan-out time.

The second technique is targeted to a core used for testing of surrounding cores. The core provides external test (EXTEST). In this case the test vectors are applied into core outputs and the responses are captured in core inputs. Therefore, the scan objects order is proposed in the following scheme: output scan cells, internal scan chains, input scan cells. The optimization is performed for balancing scan-in time and scan-out time of EXTEST.

The other two techniques are targeted to balance not scan-in time and scan-out time but the lengths of the parallel lines. One technique uses the scan object ordering for the internal and the other one for the external test.

Comparison of single optimization techniques showed advantages of each technique. If the parallel access is optimized for one test type, the application of this test type is very efficient. If a core has no preferred test type the best choice is to select one of the techniques for the lengths of the parallel lines. However, these two techniques form a compromise and the scan-in time and the scan-out time for both test types are longer than the times for optimization for one test type. This was the main reason for development of the reconfigurable optimization technique using advantages of the two single optimization techniques.

4.2 Reconfigurable optimization technique

The reconfigurable optimization technique combines the best scan-in time and scan-out time for both INTEST and EXTEST in one test wrapper. It uses single optimization techniques for INTEST and EXTEST simultaneously. The wrapper is constructed as a reconfigurable architecture where the ordering in the parallel lines depends on the test type.

The technique firstly arranges the parallel lines optimized for INTEST. In the beginning of the lines, there are input scan cells, then internal scan chains, and output scan cells. All parallel lines are balanced for scan-in time and scan-out time for INTEST. The EXTEST optimization is slightly different from the single optimization for EXTEST. In the reconfigurable architecture it is not required to connect internal scan chains in configuration for the external test. They are used only for the internal test. Therefore, the EXTEST ordering redistributes the input scan cells as well as the output scan cells in all parallel lines evenly. When Φ_i is the number of input scan cells and k the number of parallel lines, one line in EXTEST configuration contains n input cells where $n = \Phi_i/k$. In this configuration maximal difference between parallel lines lengths is 1 bit (when k is not integer divisor of Φ_i).

The difference between the two scan configurations lies not only in ordering (input cells are ordered first in parallel lines for INTEST but at the end of lines for EXTEST) but also in the numbers of scan cells and internal chains in lines. Switching between two configurations is provided by several multiplexers. The simplest way how to reconfigure is to add one additional multiplexer into each scan cell. This solution enlarges the test area in the SoC and therefore is not satisfactory. The proposed reconfigurable technique minimizes the number of multiplexers. In various test wrappers for various cores the number of multiplexers is different. The main idea is to find the longest chains of scan cells of one type. These chains are defined on the basis of both parallel line configurations. Then one multiplexer serves one chain.

An example of the reconfigurable architecture generated by the proposed technique is shown in Figure 1. The small blocks in the figure represent chains of input scan cells (pale blocks), output scan cells (black blocks), and internal scan chains. The written numbers stand for the number of scan cells of one chain. One multiplexer is connected before each block of scan cells. Configuration for the internal test (Figure 1a) is used during WP_INTEST instruction execution. Figure 1b shows configuration for the external test where the internal scan chains are not connected. The number of multiplexers in presented example is 13 instead of 85 (one multiplexer for each scan cell).

When the test wrapper with the parallel test interface is designed in accordance with IEEE 1500 standard the instruction set has to contain WP_PRELOAD instruction. The reconfigurable wrapper architecture has two configurations of parallel lines therefore new instruction has to be added. WP_PRELOAD instruction uses configuration for the internal test and new WP_PRELOAD_E instruction uses second configuration for the external test.

4.3 Experimental results

The reconfigurable optimization technique is intended to reduce scan-in time and scan-out time for internal and external tests in one test wrapper. Table 1 shows several parameters of the single technique for EXTEST (columns 2 to 7) and of the reconfigurable technique (last four columns) for different width of the parallel interface. The first column shows suggested widths of the parallel interface (it is also the number of parallel lines). Next two columns show the maximal and minimal length of parallel lines. The experiments shown in Table 1 have been made for a core with 33 input bits, 16 output bits, and 4 internal scan chains (with chains lengths: 16, 12, 8, and 6 bits). Scan-in and scan-out parameters for EXTEST are the same for both techniques for all widths of the parallel interface. But the reconfigurable technique gives better times for INTEST (scan-in and scan-out columns for INTEST) in comparison with the single optimization technique for EXTEST (scan-in and scan-out columns for INTEST).

Table 2 shows the area overhead comparison for several cores [6]. The gates numbers of the standard test wrap-

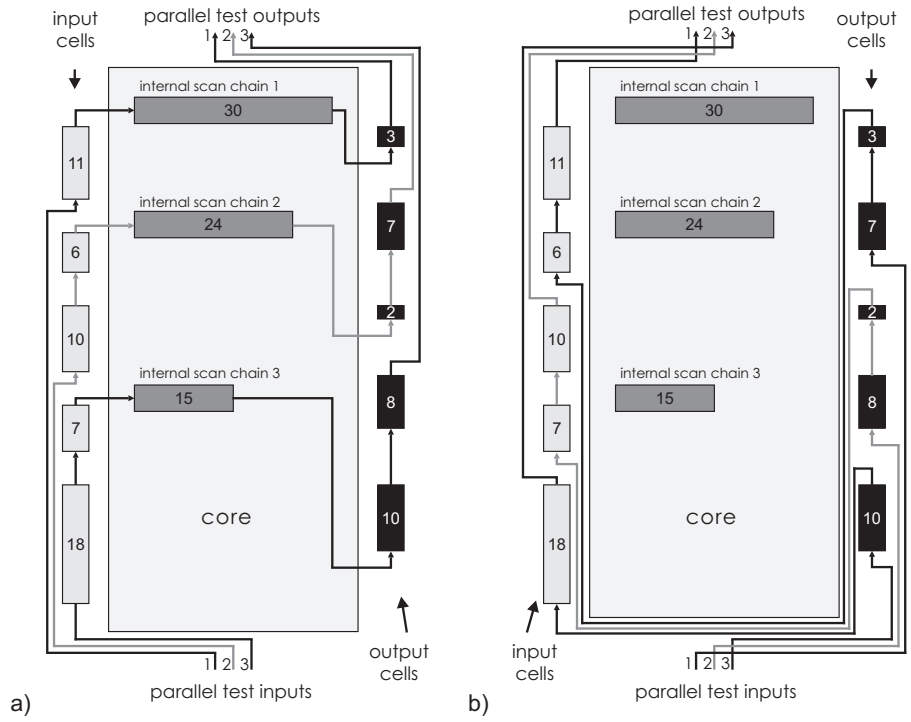

Figure 1: Reconfigurable wrapper architecture. Configuration for a) INTEST and b) EXTEST.

Table 1: Parameters of single optimization technique for EXTEST and reconfigurable optimization technique

	Optimization technique for external test						Reconfigurable optimization technique			
			INTEST		EXTEST		INTEST		EXTEST	
width	max	min	scan-in	scan-out	scan-in	scan-out	scan-in	scan-out	scan-in	scan-out
2	46	45	46	46	8	17	38	29	8	17
3	32	29	32	32	6	11	25	20	6	11
4	28	12	28	28	4	9	19	16	4	9
5	25	10	25	25	4	7	16	16	4	7
6	24	8	24	24	3	6	16	16	3	6
7	23	7	23	23	3	5	16	16	3	5
8	22	6	22	22	2	5	16	16	2	5
9	21	5	21	21	2	4	16	16	2	4
10	20	5	20	20	2	4	16	16	2	4
11	20	4	20	20	2	3	16	16	2	3
12	20	4	20	20	2	3	16	16	2	3
13	19	3	19	19	2	3	16	16	2	3
14	19	3	19	19	2	3	16	16	2	3
15	19	3	19	19	2	3	16	16	2	3

pers without parallel interface are in the second row of table. The third row gives the numbers of gates of the test wrappers with 3-bit parallel interface. The area overheads comparisons with standard test wrappers from the second row are shown in the fourth row. The areas of the reconfigurable test wrappers generated by the proposed technique are in the fifth row and the comparison with the standard wrapper in the last row. For all cores the area overhead of the reconfigurable test wrappers is less than 1% of the standard test wrapper area with the serial interface only.

5. New delay fault test generation method

The new method was developed for delay fault test generation aimed at embedded cores. The proposed method is designated for transition faults test generation with primary application through simple boundary scan chain (one memory element per one scan cell). Simple boundary

Table 2: Area overhead comparison

core	is35938	is35933	iid3s32	iigost32
standard wrapper w/o parallel interface (no. of gates)	115 022	102 504	61 638	58 295
wrapper with 3-bit parallel interface (no. of gates)	115 390	102 801	61 748	58 410
area overhead (%)	0,32%	0,29%	0,18%	0,20%
reconf. wrapper with 3-bit parallel interface (no. of gates)	115 758	103 026	61 919	58 512
area overhead (%)	0,64%	0,51%	0,46%	0,37%

scan chain occupies smaller area than enhanced boundary scan chain but for its simpler construction it is not suitable for ordinary delay fault test. Therefore, it was necessary to propose a method to generate tests for delay faults applicable through simple boundary scan chain. The method is based on skewed-load test (launch-on-shift test) for the internal scan chains and the basic principle is characterized by Strategy 1.

STRATEGY 1. *A vector-pair to detect transition faults is applied through a simple scan chain as a one bit sequence, where an excitation vector is created by one bit shift of an initialization vector.*

The basic requirements of the proposed method for the optimal test length of generated test for transition faults were (1) test application via a simple scan chain without the use of neighboring test cores (Strategy 1), and (2) the minimal test application time. The second strategy was formulated to minimize test application time.

STRATEGY 2. *The vector-pairs diagnosing the transition faults create one sequence of binary values in which each vector-pair corresponds to the strategy 1 and also two consecutive vector-pairs are generated by one or more bit shifts.*

5.1 Basic principles of the proposed method

The transition fault test consists of vector-pairs where one vector-pair covers one or more transition faults. The excitation vector of vector-pair is actually a stuck-at test vector according to basic principle of delay fault test. For this reason, the majority of existing automatic test generator for transition faults is based on test vectors for stuck-at-0 and stuck-at-1 faults.

The bit sequence formed by the random or pseudo-random vectors corresponds to Strategy 1 and 2. The length of this type of bit sequence is very long, which leads to intolerable increase of test application time for larger circuits. This solution also needs use of a fault simulator to determine the fault coverage.

The proposed method for generating a bit sequence is based on deterministic tests and thus it generates a deterministic test sequence for transition faults. However, it is not possible to use standard tests for stuck-at faults like it is used in other test generators for delay faults [7, 11, 12, 15]. Existing stuck-at tests are optimized mostly for a minimal number of test vectors. For that reason selection of appropriate vectors for transition fault test in accordance to Strategy 1 and 2 is very limited due shift dependency. Therefore, the proposed method uses modified stuck-at tests, which consists of sets of test vectors for every detectable stuck-at fault. This approach increased the probability of delay fault test generation for test Strategy 1 and 2, and also the overall coverage of delay faults.

The initialization and excitation vectors can be merged into one bit sequence if the corresponding bits are identical, or at least one of them is undefined. This condition is known as vector consistency and the bit sequence is referred to as m-vector.

DEFINITION 1. *Let $v1$ denote the initialization vector and $v2$ the excitation vector in the circuit with N inputs then $m = (m_1, m_2, \ldots m_{N+1})$ with $m_1 = v1_1$, $m_{N+1} = v2_N$ is m-vector only if m_i for $i = 2, 3, \ldots N$ is determined by one of the possibilities from the table 3.*

Table 3: Allowed bit combination for defining m-vector

$v1_i$	$v2_{i-1}$	m_i
0	0	0
0	X	0
X	0	0
1	1	1
1	X	1
X	1	1
X	X	X

M-vector is the bit sequence $N + 1$ bits long, where excitation vector ($v2$) is generated by one shift operation of the initialization vector ($v1$).

To find an appropriate initialization vector, the proposed method uses a set of excitation vectors for the second type of transition fault on the same wire. The set of excitation vectors does not cover whole set of initialization vectors for second transition fault on the same wire. Therefore, the proposed method includes simulator of initialization values. It performs two basic operations:

1. In the case that no vector from the set is suitable for m-vector creation the simulator is used to find a suitable initialization vector.
2. If there is a vector from the set, which is also an initialization vector for opposite transition fault, the simulator finds its minimal form (vector bits, which initially provide test value propagation to outputs are replaced by undefined values) and thus also provides a minimal form of m-vector.

One of the proposed method requirements is the shortest test application of the generated test sequence which is achieved only by a short generated test sequence. The length of the sequence is determined by two factors: (1) number of m-vectors in the sequence, and (2) capability to cover more transition faults by one m-vector.

The proposed method generates more m-vectors for each transition fault. Set of m-vectors for each transition fault is searched to find minimal number of m-vectors, which would cover all faults in the core. Searching the set of m-vectors starts with singular m-vectors.

DEFINITION 2. *M-vector is known as singular m-vector only if none of others m-vectors can diagnose the transition fault.*

Singular m-vector covers the transition fault as only one; therefore it must be certainly included in the generated test sequence. Application of initialization vector and excitation vector consequently creates a partial sensitive path in the core. The sensitive path is created between the primary inputs and wire where the transition fault is tested. M-vector may also cover other transition faults which occur on the sensitive path.

DEFINITION 3. *Let $ms \in S$ is singular m-vector and $m_f \in M_f$ is m-vector covering the transition fault f, if for all vector bits is $(ms_i = 0 \wedge m_{fi} \neq 1) \vee (ms_i = 1 \wedge m_{fi} \neq 0)$ for $i = 1, 2, \ldots N$, then it is considered that m-vector m_f overlaps m-vector ms.*

If the set M_f contains only one m-vector, which can overlap one singular m-vector, this overlap is performed. If the set M_f contains more vectors, which can overlap the same singular m-vector the selection of the best one is performed in several steps. The number of replaced undefined bits in the singular m-vector is considered and also overlapping m-vectors for fault f are compared with overlapping m-vectors of other faults.

If the set M_f contains no m-vector, which overlaps any singular m-vector, it is necessary to choose the representing m-vector of the set M_f. The selection of the best m-vectors for transition faults without any overlap on singulars m-vectors is made with the constraint to find the minimal number of m-vectors, which would cover all remaining faults.

The proposed method generates minimized set of m-vectors, which covers all diagnosable transition faults in the core under test. The set can be formed into one of three test types. Each type is applicable to various types of test wrapper architectures.

6. Experimental results

The proposed method for delay test generation was validated with numerous experiments. Test pattern generator Atalanta [13] was used to generate excitation vectors. This stuck-at fault generator provides generation of multiple test vectors for every fault. This feature was mandatory, since the proposed method is based on it.

Experiments were performed using combinational benchmark circuits ISCAS'85 and sequential benchmark circuits ISCAS'89 with internal scan chains. Two parameters were observed: transition fault coverage and test application time. Table 4 shows results for minimal test sequence on selected circuits. The minimal test sequence is aimed for wrapper containing simple boundary scan chains (tables with all results are placed in the thesis). For every circuit Table 4 depicts the number of m-vectors needed for transition fault test and the bit length of generated test sequence. Average distance represents the average distance of two consequent m-vectors in the generated bit order. For example, the average distance for circuit s510 is 7 bits. It means the new m-vector starts every 7^{th} bit in average. The length of m-vectors, which is $N + 1$, has also influence on average distance. The length of m-vectors for circuit s510 is 26 bits, thus one bit is in 4 m-vectors in average. Ideal case is when the distance is 1. In that case every m-vector is only one bit shift distant from previous one. In that case excitation vector of first m-vector is also initialization vector of second m-vector.

Last column of Table 4 shows compress ratio defined by the equation $(L - Lo)/L$, where Lo is length of generated test and $L = number\_of\_m - vectors * (N + 1)$. Table 4 also shows transition fault coverage. The average coverage for all shown circuits is 83.4%. All tests were generated with default ordering of core inputs. The test coverage depends also on the shift dependency; therefore it can be improved by inputs reordering.

7. Conclusions

The aim of the thesis was to improve the quality of testing of digital cores surrounded with test wrapper (1) by optimizing the parallel interface for faster test application and (2) by effective method of delay fault test generation requiring only the simple test wrapper architecture.

The developed optimization methods of the parallel interface generate parallel scan lines based on four criteria for different types of the applied test. The use of this method in the design process of test wrapper offers effective utilization of the whole width of the parallel interface. For more effective test application the reconfigurable test wrapper architecture was also developed; this architecture benefits from the simultaneous use of two optimization criteria without significant area increase. The developed optimization methods were implemented into a software tool for automatic generation of wrapper structures [5].

Another result of the thesis is the new test generation method for one delay fault model — for transition faults. The developed method is based on skewed-load test and it eliminates the disadvantage of fast scan enable signal. The generated delay fault test can be applied through test wrapper with only simple boundary scan chain; this eliminates the necessity to use the extended boundary scan chain for the application of delay fault test. The method generates three types of tests, for which the methodology of their application for different test wrapper architectures was designed; by this the method gained on universality.

The effectiveness of the developed method for transition delay test generation was verified on the selected set of combinational and sequential circuits. The experiments show significant reduction of test vector application time for delay faults in comparison with other recently published transition test methods for embedded digital cores. The generated tests require only simple test wrapper architecture for the delay fault test.

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Table 4: Experimental results for wrapper containing simple boundary scan chains

circuit	number of PI + PPI	number of m-vectors	length of test sequence [bit]	transition faults coverage	average distance [bit]	compress ratio [%]
c17	5	7	18	82.4%	2.6	57.1%
c432	36	201	2874	87.6%	14.3	61.4%
c499	41	245	6198	71.3%	25.3	39.8%
c880	60	203	7523	85.0%	37.1	39.2%
c1355	41	545	17565	59.8%	32.2	23.3%
c1908	33	739	16596	82.1%	22.5	33.9%
c2670	233	545	46038	95.3%	84.5	63.9%
c3540	50	801	12905	73.6%	16.1	68.4%
c5315	178	1690	96327	87.3%	57.0	68.2%
s208	19	51	461	82.7%	9.0	54.8%
s298	17	29	201	83.7%	6.9	61.5%
s344	24	51	614	92.2%	12.0	51.8%
s349	24	48	627	92.3%	13.1	47.8%
s382	24	46	473	86.1%	10.3	58.9%
s400	24	43	433	86.1%	10.1	59.7%
s420	35	94	1763	81.4%	18.8	47.9%
s444	24	53	504	85.8%	9.5	62.0%
s510	25	80	562	85.9%	7.0	73.0%
s526	24	85	914	85.6%	10.8	57.0%
s526n	24	82	906	86.0%	11.0	55.8%
s641	54	81	2196	93.0%	27.1	50.7%
s713	54	84	2196	92.3%	26.1	52.5%
s832	23	119	854	71.3%	7.2	70.1%
s838	67	152	4624	80.3%	30.4	55.3%
s953	45	162	1738	82.9%	10.7	76.7%
s1196	32	238	2443	80.3%	10.3	68.9%
s1238	32	255	2450	79.0%	9.6	70.9%
s1423	91	220	13462	90.2%	61.2	33.5%
s1488	14	140	917	81.6%	6.6	56.3%
s1494	14	146	864	81.6%	5.9	60.5%
s5378	214	430	40871	80.6%	95.1	55.8%

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